[0049] What is claimed is:

1. A method comprising:

translating a first sequence of instructions associated with a source architecture into a second sequence of instructions associated with a target architecture,

wherein said first sequence includes one or more floating point control instructions and said second sequence does not include a floating point control instruction, and

wherein results produced by executing said second sequence on a processor that complies with said target architecture are substantially the same as results produced by executing said first sequence on a processor that complies with said source architecture.

2. The method of claim 1, wherein said second sequence includes an instruction to round an initial floating point number to a first floating point number using round to zero rounding mode, regardless of a rounding mode setting of the target architecture.

3. The method of claim 1, wherein said first sequence of instructions and said second sequence of instructions are binary code.

4. The method of claim 1, further comprising:

identifying in said first sequence a rounding mode of one of said one or more floating point control instructions.

5. A method comprising:

translating a first sequence of instructions associated with a source architecture into a second sequence of instructions associated with a target architecture,

wherein said first sequence includes an instruction to save a first rounding mode, followed by an instruction to set a second rounding mode that is not round to zero, followed by an instruction to generate an integer number by rounding an initial floating point number according to said second rounding mode, followed by an instruction to set said first rounding mode,

wherein said second sequence includes an instruction to generate a first floating point number by rounding to zero said initial floating point number, and

wherein results produced by executing said second sequence on a processor that complies with said target architecture are substantially the same as results produced by executing said first sequence on a processor that complies with said source architecture.

6. The method of claim 5, wherein said second sequence further includes an instruction to compare a value of said first floating point number to a value of said initial floating point number.

7. The method of claim 6, wherein said second rounding mode is a round toward positive infinity mode, and said second sequence further includes an instruction to add one to said first floating point number in the event that said first floating point number is not negative and the value of said first floating point number is not equal to the value of said initial floating point number.

8. The method of claim 6, wherein said second rounding mode is a round toward negative infinity mode, and said second sequence further includes an instruction to subtract one from said first floating point number in the event that said first floating point number is not positive and the value of said first floating point number is not equal to the value of said second floating point number.

9. A method for converting a floating point representation to an integer representation with a round to negative infinity rounding mode, the method comprising:

using a round to zero forced mode instruction to convert an initial floating point number to a first floating point number; and

if said first floating point number is not positive, and a value of said first floating point number is not equal to a value of said initial floating point number, generating a second floating point number by subtracting one from said first floating point number, and generating said integer representation by converting the floating point representation of said second floating point number to an integer representation.

10. The method of claim 9, further comprising:

if said value of said first floating point number is equal to said value of said initial floating point number, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

11. The method of claim 9, further comprising:

if said first floating point number is positive, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

12. A method for converting a floating point representation to an integer representation with a round to positive infinity rounding mode, the method comprising:

using a round to zero forced mode instruction to convert an initial floating point number to a first floating point number; and

if said first floating point number is not negative, and a value of said first floating point number is not equal to a value of said initial floating point number, generating a second floating point number by adding one to said first floating point number, and generating said integer representation by converting the floating point representation of said second floating point number to integer representation.

13. The method of claim 12, further comprising:

if said value of said first floating point number is equal to said value of said initial floating point number, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

14. The method of claim 12, further comprising:

if said first floating point number is negative, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

15. An article comprising a storage medium having stored thereon instructions that, when executed by a computing platform, result in:

translating a first sequence of instructions associated with a source architecture into a second sequence of instructions associated with a target architecture,

wherein said first sequence includes one or more floating point control instructions and said second sequence does not include a floating point control instruction, and

wherein results produced by executing said second sequence on a processor that complies with said target architecture are substantially the same as results produced by executing said first sequence on a processor that complies with said source architecture.

16. The article of claim 15, wherein said second sequence includes an instruction to round an initial floating point number to a first floating point number using round to zero rounding mode, regardless of the rounding mode setting of the target architecture.

17. The article of claim 15, wherein the instructions further result in:

identifying in said first sequence a rounding mode of one of said one or more floating point control instructions.

18. An article comprising a storage medium having stored thereon instructions for conversion of a floating point representation to an integer representation with a round to negative infinity rounding mode, wherein the instructions, when executed by a computing platform, result in:

using a round to zero forced mode instruction to convert an initial floating point number to a first floating point number; and

if said first floating point number is not positive, and a value of said first floating point number is not equal to a value of said initial floating point number, generating a second floating point number by subtracting one from said first floating point number, and generating said integer representation by converting the floating point representation of said second floating point number to an integer representation.

19. The article of claim 18, wherein the instructions further result in:

if said value of said first floating point number is equal to said value of said initial floating point number, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

20. The article of claim 19, wherein the instructions further result in:

if said first floating point number is positive, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

21. An article comprising a storage medium having stored thereon instructions for conversion of a floating point representation to an integer representation with a round to positive infinity rounding mode, wherein the instructions, when executed by a computing platform, result in:

using a round to zero forced mode instruction to convert an initial floating point number to a first floating point number; and

if said first floating point number is not negative, and a value of said first floating point number is not equal to a value of said initial floating point number, generating a second floating point number by adding one to said first floating point number, and generating said integer representation by converting the floating point representation of said second floating point number to integer representation.

22. The article of claim 21, wherein the instructions further result in:

if said value of said first floating point number is equal to said value of said initial floating point number, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

23. The article of claim 21, further comprising:

if said first floating point number is negative, generating said integer representation by converting the floating point representation of said first floating point number to an integer representation.

24. An apparatus comprising:

a memory device; and

a processor to translate a first sequence of instructions associated with a source architecture into a second sequence of instructions associated with a target architecture,

wherein said first sequence includes one or more floating point control instructions and said second sequence does not include a floating point control instruction, and

wherein results produced by executing said second sequence on a processor that complies with said target architecture are substantially the same as results produced by executing said first sequence on a processor that complies with said source architecture.

25. The apparatus of claim 24, wherein said processor is to translate said first sequence into said second sequence so that said second sequence includes an instruction to round an initial floating point number to a first floating point number using round to zero rounding mode, regardless of the rounding mode setting of the target architecture.

26. The apparatus of claim 24, wherein said processor is to identify in said first sequence a rounding mode of one of said one or more floating point control instructions.